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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,492	03/01/2004	Nobuaki Hashimoto	118876	9029

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/788,492	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	Matthew C. Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10,12 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,12 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 20 is objected to because of the following informalities: the limitation "interconnect patter" in line 2 of the claim should be changed to "interconnect pattern". Appropriate correction is required.

Terminal Disclaimer

The terminal disclaimer filed on September 13, 2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of Application No. 10/788449 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung et al. (US Pat. 6,747,348, hereinafter Jeung) in view of Ling et al. (US Pat. 6,445,069, hereinafter Ling).

Regarding claim 20, Figure 4L of Jeung discloses a substrate 24 on which an interconnect pattern is formed; a chip component 22 that has a base material, the chip component having a first surface on which a pad 21 is formed and a second surface opposite to the first surface, the

chip component being mounted in such a manner that the second surface faces the substrate; an insulating section 42 (portions on the side of the chip) that has a first portion disposed on the upper surface of the chip and a second portion disposed adjacent to the chip component, the insulating section having a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken, the convex surface ascending from the first surface to have a top surface and descending from the top surface in an outward direction, the first portion having a lower surface than the top surface, the insulating section having an edge disposed between the pad and a part of the periphery of the chip component on which the insulating section is disposed, the edge being closest of the insulating section to the pad, and an interconnect 49 that is formed to extend from above the pad to above the interconnect pattern, the interconnect having a second section disposed over the insulating section, the interconnect covering all lateral surfaces of the pad.

Jeung does not disclose a metal layer formed of a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion preventing layer preventing any diffusion of material formed thereabove into the base material of the chip component. Ling discloses a chip component 10 of a base material having a first surface on which a pad 26 is formed and metal layer 32/34/36 formed of a plurality of layers including a diffusion prevention layer 32/34 in contact with the pad and an uppermost layer 36 being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Jeung by forming a metal layer such as that taught by Ling. The

motivation for doing so is to allow the use of copper interconnect metallization while facilitating the electrical coupling of connection pads to supporting substrates or other packaging while using known metal deposition processes in a simple and inexpensive manner that is compatible with gold bond wires, solder bumps, and other common circuit connection methods and that allows tight spacings between adjacent connections pads without compromising the reliability of the integrated circuit.

Further, Jeung does not disclose a passivation layer on the first surface of the chip component. However, Ling teaches a passivation layer 13 over the chip where the metal layers (electrode), are exposed through the passivation layer. At the time of the invention it would have been obvious to one of ordinary skill in the art to form a passivation layer over the chip. The reasons for forming a passivation layer are well known in the art, including to passivate and protect the surface of the layers of the chip. In combination, the insulating section has a portion on the passivation layer since the insulating section of Jeung covers a top surface of the chip. Further, the interconnect will have a first section disposed on the passivation film since the interconnect is formed on the upper surface of the chip.

Claims 1, 4, 5, 12, and 17-20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung et al. (US Pat. 6,750,547, hereinafter Jeung'547) in view of Ling and Jeung.

Regarding claims 1, 5, and 20, Figure 1G of Jeung'547 discloses a substrate 120 on which an interconnect pattern is formed; a chip component 130 that has a base material, the chip component having a first surface on which a pad 133 is formed and a second surface opposite to

the first surface, the chip component being mounted in such a manner that the second surface faces the substrate; a passivation film 134 that is formed on the first surface of the chip component, the passivation film formed to avoid at least a part of the pad; an insulating section 135 that has a first portion disposed on the passivation film and a second portion disposed adjacent to the chip component, the insulating section being formed to come to an end at a position a distance away from the metal layer, the first portion having a lower surface than the top surface, and an interconnect 49 that is formed to extend from above the pad to above the interconnect pattern, the interconnect having a first section disposed on the passivation film and a second section disposed over the insulating section, the interconnect covering all lateral surfaces of the pad. Regarding claim 20, Figure 1G of Jeung'547 further discloses the insulating section having an edge disposed between the pad and a part of the periphery of the chip component on which the insulating section is disposed, the edge being closest of the insulating section to the pad. Regarding claim 5, the above device must be made by the claimed method.

Jeung'547 does not disclose a metal layer formed of a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion preventing layer preventing any diffusion of material formed thereabove into the base material of the chip component. Ling discloses a chip component 10 of a base material having a first surface on which a pad 26 is formed and metal layer 32/34/36 formed of a plurality of layers including a diffusion prevention layer 32/34 in contact with the pad and an uppermost layer 36 being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component. In view of such teaching, it would have been obvious to the ordinary artisan at the

time the invention was made to modify the invention of Jeung by forming a metal layer such as that taught by Ling. The motivation for doing so is to allow the use of copper interconnect metallization while facilitating the electrical coupling of connection pads to supporting substrates or other packaging while using known metal deposition processes in a simple and inexpensive manner that is compatible with gold bond wires, solder bumps, and other common circuit connection methods and that allows tight spacings between adjacent connections pads without compromising the reliability of the integrated circuit.

Jeung'547 does not explicitly disclose the insulating section having a convex surface. However, Jeung'547 discloses the insulating section 135 can be formed using a viscous type of dielectric material (col. 4, lines 18-25). When using this type of dielectric material, the dielectric layer 135 would not have the sharp corners shown in Figure 1G, unless some other etching/shaping process was performed (which Jeung'547 does not disclose). Clearly, Figure 1G is just a simplified diagram and does not represent the real world actuality. In reality, the corners would be more rounded and therefore have the convex shape claimed. Regardless, Figure 4L of Jeung specifically discloses an insulating section 42 having the claimed convex shape. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Jeung'547 by using the convex shape taught by Jeung for the insulating section for at least the purpose of simplifying the production process (since no additional etching/shaping process would be required, as is required to obtain the sharp corners shown in Figure 1G of Jeung'547). Furthermore, the mere change in shape recited in the claims is considered obvious to one of ordinary skill in the art as it requires only a minor modification of the shape in Jeung'547 that does not result in any difference in operation or effect. *In re*

Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966) (The court held that the configuration of the claimed disposable plastic nursing container was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the claimed container was significant.).

Regarding claims 4 and 12, Figure 2E of Jeung'547 discloses a connecting layer 124 disposed between the chip component and the substrate, wherein the insulating section is formed of the same material (oxide) as the connecting layer (col. 3, lines 3-5 and col. 4, lines 11-13).

Regarding claim 17, Figure 2E of Jeung'547 discloses a printed circuit board 180 on which the electronic device of claim 1 is mounted.

Regarding claim 18, the device of Jeung'547 is considered an electronic instrument.

Regarding claim 19, Figure 1G of Jeung'547 discloses a part of the passivation film 134 on which the first section of the interconnect is disposed being between the pad 133 and the insulating section 135.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung'547 in view of Ling and Jeung as applied to claim 5 above, and further in view of Ito et al. (US Pat. 6,625,032, hereinafter Ito).

With regard to claims 6 and 7, a further difference between Jeung'547 and the claimed invention is the interconnect being formed of a dispersant including electrically conductive particles or forming the layer includes ejecting the material over the metal layer, the insulating section, and the interconnect pattern. Ito et al. teach on column 1 lines 30-37 that a dispersant

including electrically conductive particles is ejected onto a substrate to form conductive layers. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the prior art conductive particles in dispersant ejecting method of Ito et al. in the method of Jeung'547 to obtain rapid implementation of interconnects on surfaces.

Claims 2 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung'547 in view of Ling and Jeung, or over Jeung'547 in view of Ling, Jeung, and Ito as applied to claims 1, 5, 6, and 7 above, and further in view of Tanabe (JP 01-164044).

Regarding claims 2 and 8-10, Jeung'547 does not specifically disclose the insulating section being formed of resin. Tanabe discloses forming an insulating section in a configuration similar to that of Jeung'547 in that it is formed on the substrate 1 and along the side of the chip 4 to surround the chip. Tanabe discloses the insulating section being formed of resin. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of to employ a resin as taught by Tanabe for the insulating section of Jeung'547. It has been held that the use of conventional materials to perform their known functions in a conventional process is obvious. *In Re Raner* 134 USPQ 343 (CCPA 1962). Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In Re Leshin*, 15 USPQ 416.

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

However, it should be noted that Applicant argues, "On the contrary, the recited configuration of the convex surface are significant, as described, for example, on page 13, line 18 – page 14, line 6, of Applicant's specification, as filed". However, the portion of the specification cited by Applicant does not mention any advantage or reason for having the convex shape.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is 571-272-1731. The examiner can normally be reached on 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew C. Landau
Primary Examiner
Art Unit 2815
12/5/07